What is claimed is:

1. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming first and second well each having a n-type conductivity in a semiconductor substrate,

(b) forming third and fourth well each having a p-type conductivity in the semiconductor substrate;

(c) forming a first gate insulation film on the first well, a second gate insulation film on the second well, a third gate insulation film on the third well and a fourth gate insulation film on the fourth well, wherein the first and third gate insulation film are thicker than the second and fourth gate insulation film;

(d) applying oxynitridation to the first, second, third and fourth gate insulation film;

(e) forming a first gate electrode of a first MISFET on the first gate insulation film, a second gate electrode of a second MISFET on the second gate insulation film, a third gate electrode of a third MISFET on the third gate insulation film and a fourth gate electrode of a fourth MISFET on the fourth gate insulation film;

(f) implanting an ion that contains nitrogen or nitrogen atoms, using a resist mask having a opening at a forming region of the third MISFET, and after the step (e); and

(g) forming a first extention region of the first MISFET, a second extention region of the second MISFET, a third extention region of the third MISFET, and a fourth extention region of the forth MISFET, after the step (f).

2. A method of manufacturing a semiconductor device according to claim 1, wherein the first step (c) comprises the step of:

oxidizing a surface of the semiconductor substrate;

removing a oxide film formed in a forming region of the second and fourth MISFET; and

re-oxidizing a surface of the semiconductor substrate.

3. A method of manufacturing a semiconductor device according to claim 1, wherein the first and second extention region are a p-type semiconductor region, and the third and fourth extention region are a n-type semiconductor region.

4. A method of manufacturing a semiconductor device according to claim 3, further comprising the step of:

(h) forming a sidewall spacer on the side of the first, second, third and fourth gate electrode, after the step (g); and

(i) forming a p^+ type semiconductor region of the first and second MISFET, and a n^+ type semiconductor region of the third and fourth MISFET, after the step (h).

5. A method of manufacturing a semiconductor device according claim 4, wherein the first and second MISFET are a p-channel type MISFET, the third and fourth MISFET are a n-channel type MISFET, the first and third MISFET are a high voltage MISFET, and the second and fourth MISFET are a low voltage MISFET.